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MICROWAVE SEMICONDUCTOR RESEARCH-MATERIALS, DEVICES, CIRCUITS. (U)
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6/1/78 - 4/30/79

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MICROWAVE SEMICONDUCTOR RESEARCH-

MATERIALS, DEVICES, CIRCUITS

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Chromium doped pure LPE GaAs buffer layers have been tested to show that they do not conduct after baking with or without Si_3N_4 capping, and calibrated deep level transient spectroscopy has been used to measure the density of intended chromium traps as $3-4 \times 10^{14}/cm^3$.

Technology for obtaining quasi-Schottky barrier gates on quaternary compound semiconductor materials has been developed.

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A review of the entire field of Schottky barriers on compound semiconductors has been performed, and the results published.

Two-dimensional numerical analyses have enhanced the understanding of the physical basis of MESFET operation. The influence of such materials parameters as shape of the velocity-field curves and nature of the diffusivity-field characteristics on parasitic elements in MESFET's has been determined. Expected performance of silicon, GaAs, and InP short-channel MESFET's has been compared.

High power GaAs FET drain voltage breakdown has been extended to about 50 V and the Electric field geometry has been measured to show a Gunn domain with thickness and shape consistent with theory. Substrate parasitic space charge limited current has been analytically shown to strongly contribute to output conductance.

An integrated computer-aided-design approach for microwave GaAs FET amplifiers has been developed for the design of wide classes of these devices. Interactive programs have been developed for the synthesis of both lumped and distributed matching networks for the design of broadband low-noise and high-power MESTET amplifiers.

Coaxial IMPATT reflection amplifiers with constant voltage bias have been built at x band. These amplifiers have linear output power as a function of input power, and very low intermodulation distortion.

IMPATT diode design will be facilitated by measurements of intrinsic avalanche response time in Si, GaAs, Ge, and InP which were completed during this year.

Complimentary ion-implanted $n^+p\pi p^+$ silicon Read diodes were fabricated and analyzed. It was demonstrated the intrinsic response time could be increased by a factor of three compared to the $p^+n\nu n^+$ structure, giving a significant improvement in the avalanche phase delay.

A symmetry analysis of periodic wave guides with symmorphic space groups was developed. This analysis is useful for periodic structures containing axielly magnetized gyrotropic media, such as ferrites, and for charge particle beams drifting parallel to a wave guide axis.

A new and versatile technique of broad banding that is applicable to both active and passive components has been generalized and extended to new applications. This generalization facilitates the design of band-pass structures.

TABLE OF CONTENTS

WORK STATEMENT

1. Use liquid phase epitaxial techniques to achieve repeatable properties of GaAs and InP microwave device layers; and use measurement techniques such as c-v profiling, Hall measurements, and photoluminescence to characterize the grown layers.

2. Use advanced techniques, including electron beam pattern delineation and ion implantation doping, in the fabrication of high performance microwave field effect transistors.

3. Measure, obtain an understanding, and extend the limits of power field effect transistors.

4. Investigate the large signal properties of GaAs microwave field effect transistors both experimentally and theoretically over a broad range of frequencies.

5. Study the secondary multiplication properties of submicron implanted layers in silicon and GaAs as a function of implanted impurity, energy, dosage, and annealing schedule.

6. Design and fabricate a high efficiency complementary Read type silicon diode ($n^+p\pi p^+$).

7. Develop symmetry analysis methods applicable to periodic structures for microwave, millimeter, or optical devices and systems.

8. Apply the general circuits viewpoint to the practical systems of microstrip and dielectric wave guide components; and apply the circuit aspects of broadbanding to high frequency distributed structures.

9. Develop analytical and computer-aided techniques for the design of GaAs FET amplifiers with multi-octave bandwidths, broadband high-power GaAs FET amplifiers, and monolithic GaAs FET circuits and subsystems.

TASK 1 Effective Control of Compound Semiconductor Growth for High Performance Microwave Devices - Prof. Lester F. Eastman and David Woodard

Introduction:

The growth, characterization, and device suitability of Cr doped semi-insulating buffer layers grown by liquid phase epitaxy has been investigated. Empahsis was placed on quantitative determination of the Cr deep acceptor density and the Cr distribution coefficient as a function of growth temperature. The result, combined with SIMS measurements of Cr redistribution after annealing done at other laboratories, suggests a new model for the mechanism of conversion experienced by some substrate materials. The stability of semi-insulating epitaxial layers under heat treatment has been investigated.

Progress:

The Cr deep acceptor level in GaAs is a fairly strong hole trap. The capacitance transients it produces in diodes on n-type material are difficult to detect by standard Deep Level Transient Spectroscopy (DLTS). Optical DLTS can readily detect hole trapping in n-material, but quantitative measurements are possible only with a knowledge of the ratio of optical emission rates for electrons and holes. Using a combination of standard DLTS on p-type material and optical DLTS on both n and p type material, both grown by LPE including Cr as dopant, the ratio of optical emission rates has been determined for the Cr level. Using the measured ratio, quantitative measurement of the Cr deep acceptor density in n-type LPE material was done by optical DLTS and the

result compared to Hall measurements of the amount of compensation introduced by the Cr doping. Results of the DLTS and Hall measurements are in good agreement indicating that the compensation observed in Hall measurements is due solely to the deep acceptor level and is not complicated by any other acceptor or donor levels due either to Cr or possible impurities included with the Cr.

The distribution coefficient for the Cr deep acceptor level was measured at two different growth temperatures and is shown in Figure 1 along with the value obtained by others at the stoichiometric melt temperature. Growth of the eiplayers was accomplished from a melt containing about 0.8 at % Cr. The resulting deep acceptor density was 3.0×10^{14} at an average growth temperature of 685°C and 7.5×10^{14} at 747°C. It is believed that these values are very near the solubility limit. Thus, the curve of Figure 1 may actually represent the temperature dependence of the solubility. It is interesting to note that, in recent measurements of the redistribution after anneal of Cr in bulk grown crystals(1-3), the Cr concentration near the surface is found to drop to a value which is near the solubility predicted at the anneal temperature by Figure 1. Thus the surface conductivity conversion of certain Cr doped ingots may result from the Cr concentration near the surface relaxing under anneal to its solubility limit at the anneal temperature. If the background donor concentration for the crystal is above that limit the surface layer becomes conducting. This would suggest that

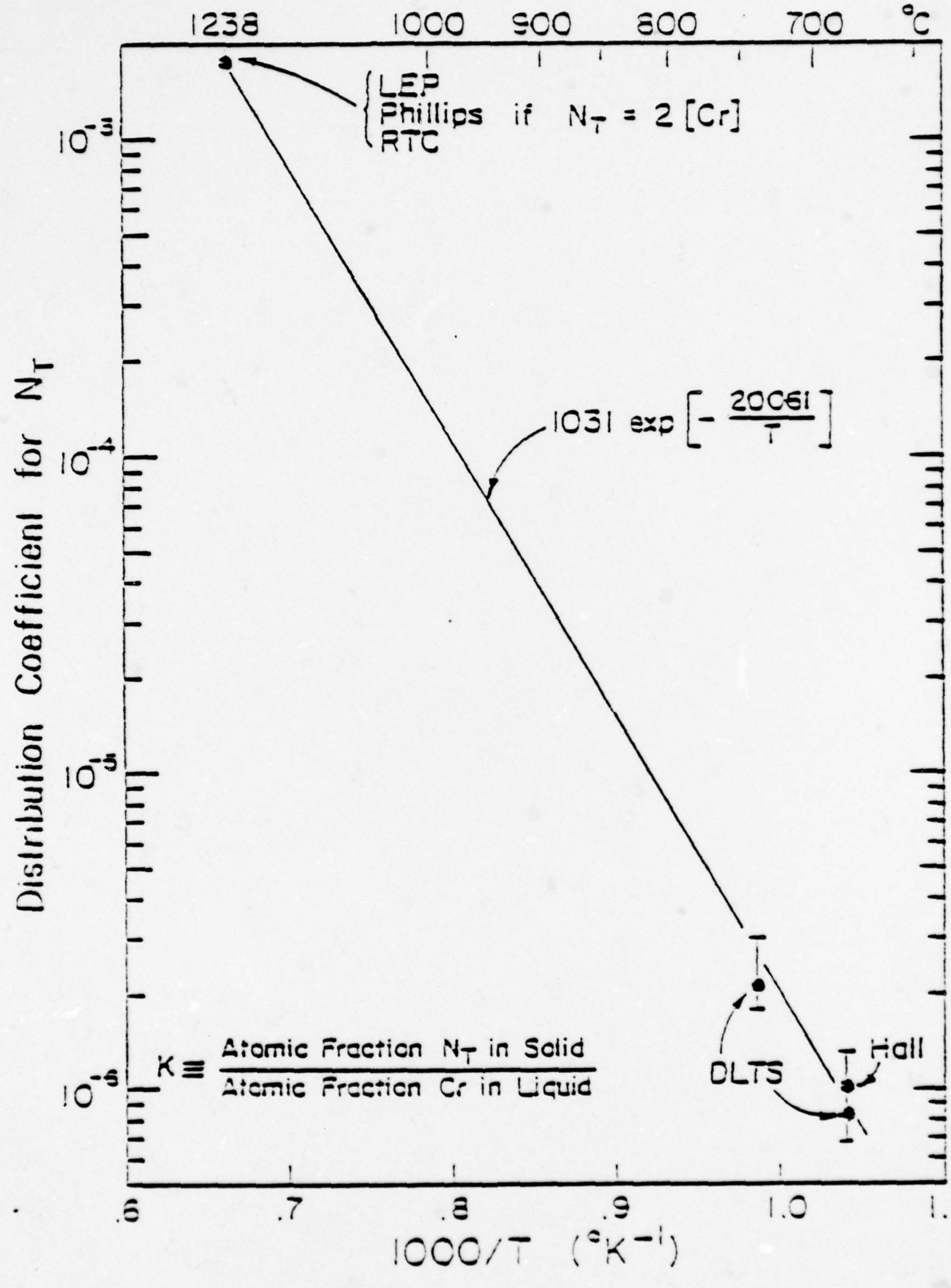

Figure 1. Distribution Coefficient of the Cr Deep Acceptor Concentration as a Function of Temperature.

epitaxial material, which is grown at a relatively low temperature where Cr solubility is low, will not convert when annealed further at the growth temperature or higher. This has been confirmed for the LPE grown material for baking time of 20 hours at 710°C in flowing H_2, and 1/2 hr at 850°C with Si_3N_4 cap.

References:

1. A. M. Huber, G. Morillot, N. T. Linh, P. N. Favennec, B. Deveaud, B. Toulouse. "Cr Profiles after Annealing with a Si_3N_4 Encapsulant". To be published in Applied Physics Letters.

2. C. A. Evans, Jr., and V. R. Leline, "Redistribution of Cr upon Post Implant Annealing of Se Implanted GaAs", IEEE 37th Annual Device Research Conference, Boulder, Colorado, June, 1979 Proceedings Unpublished.

3. D. Asbeck, J. Tandon, E. Babcock, B. Welch, C. A. Evans, Jr., and V. R. Deline, "Efforts of Cr Redistribution on Device Characteristics in Ion-Implanted GaAs IC's Fabricated with Semi-Insulating GaAs", IEEE 37th Annual Device Research Conference, Boulder Colorado, June 1979 Proceedings Unpublished.

Publications on this Task:

1. "Chromium Doped Semi Fusulating Gallium Arsenide Grown by Liquid Phase Epitaxy", D. W. Woodard, thesis, Cornell University, June 1979.

Publications in Related Areas

1. "Surface and Interface Depletion Corrections to Free Carrier Density Determinations by Hall Measurements", A. Chandra, C. E. C. Wood, D. W. Woodard, L. F. Eastman, accepted for publication in Solid State Electronics.

Talks on this Task:

"Cr Doped Semi Insulating Buffer Layers for FET's Grown by L.P.E.", D. W. Woodard and L.F. Eastman, WOCSEMMAD, Atlanta, February 1979.

Talks on Related Areas

"The Use of AlGaAs Buffer Layers to Reduce Parasitic Space Charge Limited Current Flow Through Substrates in FET Structures", L.F. Eastman, D.W. Woodard, A. Chandra and M. Shut, WOSEMMAD, Atlanta, Feb. 1979.

Information/Technology Transfer

LPE epitaxial material with semi-insulating buffer layers has been provided to Narda Microwave Corporation for fabrication into FET devices and evaluation of the process for commericial production.

Following our presentation at WOCSEMMAD, Feb. 1979, Hewlett Packard Corporation started development of Cr doping in LPE for buffer layers.

A program for investigating the use of Cr doped LPE buffer layers for implantation and fabrication into GaAs integrated circuits has been initiated at Cornell by IBM, Federal Systems Division, with the eventual objective of complete transfer of the technology.

Task 2. Materials and Processes for Microwave Field-Effect Transistors - Jeffrey Frey

Significant progress was made during the year in both the technology and the understanding of the physics of compound-semiconductor Schottky-Barrier field-effect transistors (MESFET's).

The major technological achievement was in the determination of a method of obtaining quasi-Schottky barriers on compound semiconductors, such as GaInAsP, which have a small band gap and which, consequently, exhibit very small barrier heights unless special metal/semiconductor fabrication techniques are developed. This work resulted in the publication of a useful review article on metal/semiconductor contacts in general, as well as in two publications containing specific results.

Briefly, it was shown experimentally (and confirmed by a simple theoretical approach) that very thin (<100 Angstroms) interfacial oxide layers may be used to increase the effective barrier height of Au/InP and Au/GaInAs Schottky barriers. The results, which confirmed earlier studies on Inp, extended the technique to GaInAs, and showed how it could be extended to GaInAsP, are expected to be of great use in the fabrication of MESFET's made of all these materials. In the experiments, barrier height on a specific sample of GaInAs was increased from about 0.2eV to .49eV through use of a 50 Angstrom oxide layer between metal and semiconductor.

Breakdown voltages of oxides produced by various methods were also studied; chemically deposited (CVD) oxides were shown to be best of the various types available.

Two-Dimensional device modeling work, which in our approach includes all hot-electron effects usually neglected (e.g., tensor and field-dependent nature of high-field diffusivity) in such work except velocity overshoot, resulted in a much-enhanced understanding of the relative performance of Si, GaAs, and InP MESFET's, through greater understanding of the device physics which leads to high-frequency limitations and to parasitic elements.

In the two-dimensional analysis it was shown, among other things, that the large drain-gate conductance exhibited by experimental InP devices (and which greatly hampered their high-frequency performance) was probably an effect of substrate conduction; if the substrate were perfectly insulating, InP devices should have much smaller drain-gate parasitic capacitance than GaAs devices, at large values of drain voltage (of the order of 5V for 1 micron gate devices). On the other hand, large drain-gate conductance is unavoidable over certain, lower, voltage ranges due to the large velocity dropback, and large value of high-field diffusion constant, in this material. Drain conductance was also shown to be sensitive to the value of Schottky barrier height, which is smaller in InP than in GaAs.

Drain-gate conductance was also shown, using the two-dimensional analysis, to be dependent upon substrate conduction,

through the influence of the latter on the field magnitudes achievable in the FET channel. With perfect substrates, this parasitic element should be smaller in InP than in GaAs.

Electron transit time through the channel, which affects maximum high-frequency performance, was shown to depend more on the shape of the velocity-field characteristic than on the value of low-field mobility; thus, InP, which has a mobility about half that of GaAs but a much higher peak electron velocity which, significantly, extends over a wider range of fields than that in GaAs, should have considerably better high-frequency performance, for a certain range of gate lengths and drain voltages, than GaAs.

Papers Published on Contract - May 1, 1978 - April 31, 1979

1. "Effects of Negative Differential Mobility and Magnitude of Performance of GaAs and Si FET's, R. Dawson and J. Frey, Solid State Electronics, 22, 343 (1979).

2. "Increasing the Effective Barrier Height of Schottky Contacts to n-$In_xGa_{1-x}As$", D.V. Morgan and J. Frey, Elec. Letters, 14, 737 1978.

3. "Remediable and Nonremediable Causes of Parasitic Elements in InP MESFET's", T. Wada and J. Frey, Elec. Letters, 14, 830 (1978).

4. "Physical Basis of MESFET Operation", T. Wada and J. Frey, IEEE Trans. Electron Devices, ED-26, 476 (1979)

5. "Mobility, Transit Time, and Transconductance in Submicron-Gate MESFET's", T. Wada and J. Frey, Elec. Letters, 15, 26 (1979)

6. "The Modification of Effective Metal-Semiconductor Barrier Heights by Interfacial Oxides", D.V. Morgan and J. Frey, Physica Status Solidi, 51, K23 (1979.

Papers Presented - May 1, 1978 - April 31, 1979

1. "High-Field Electron Transport in MESFET's". Invited Paper presented at IBM Research Laboratories, Yorktown Heights, July 20, 1978.

Papers Presented - May 1, 1978 - April 31, 1979 (contiued)

2. "Merging of Microwave and Digital Technologies". Invited Paper, EASCON, Washington, DC, September 27, 1978.

3. "Fundamental Material Properties and Substrate Technology: Effects on Compound Semiconductor FET Performance", T. Wada, J. Frey, J. Faricelli, - presented at 1978 IEDM, December 1978.

Technology Transfer

Technology and the results of analyses performed under this project heading are now in use in the following locations:

1. Technology for the production of quasi-SCHOTTKY-BARRIER GATES on COMPOUND SEMICONDUCTORS (InP, GaInAsP, etc.) has been the subject of wide interest among experimenters in the field, as can be judged by the large number of requests for reprints received.

2. The results of TWO-DIMENSIONAL ANALYSIS OF SHORT-CHANNEL MESFET's have also excited wide interest. Some industries have begun work on short-channel Si MESFET's due partially to the results of these analyses; such industries include Texas Instruments, Tektronix, Burroughs, and Xerox Microelectronics. At least one microwave device laboratory (Varian Associates) has been reassessing its original conclusions on the viability of InP MESFET's compared to GaAs devices, on the basis of the conclusions obtained in this project section on the performance to be expected of InP devices.

Task 3. Investigation of Microwave Field-Effect Transistor Performance Limits Set by Layer Composition and Contact Geometry - Lester F. Eastman

Introduction

Limits of performance of microwave power FET devices have been pursued with both experimental and analytical efforts. The limit of drain voltage at breakdown has been extended, and the geometry of the high field region has been measured. Use has been made of the 10:1 reduction mask aligner to delineate patterns for single-finger test channels and power FET's.

Progress

The breakdown that first occurred, at high drain voltages, at mesa steps, and the channel entrance of the gate from the bonding pad, were eliminated by design changes reducing localized fields. The breakdown voltage of the best, single-finger samples then increased to near 50V for lower currents, as shown in figure 3-1. The normalized channel current of these devices could go up to nearly .33A/mm with forward bias on the gate. When pushed to failure, damage occurred to be nearly uniform along the channel on the drain side of the device. The best devices could yield about 50-55V breakdown at .100A/mm, which matches the state of the art obtained at Bell Laboratories, for the doping involved, $4X10^{16}/cm^3$, with similar channel lengths.

The geometry of the high field layer was measured by auger excitation of unintentional ambient carbon atoms on the channel surface.

The high field was located on the drain side of the gate, in a "Gunn" domain that was more than one micron thick and with about 50,000V/cm maximum field, when 6V was applied between source and drain and .15-.20 A/mm current was flowing. This high-field Gunn domain, stationary on the drain side of the gate, was predicted by our theory. The changes in the field shape as the domain is eliminated at pinch of the device are not yet measured, but represent an important area of study. The change to higher breakdown voltage is evident below one eighth of full channel current on Figure 3-1.

The study of the contribution of space charge limited parasitic buffer/substrate current was made also. The current flow in the buffer/substrate was found to depend on (drain voltage)$^{\frac{1}{2}}$ and (channel doping)$^{\frac{1}{4}}$. This current is now believed to contribute most of the output conductance at lower instantaneous current values. It contributes to D.C. power, is a microwave parasitic lead but does not contribute substantially to the transconductance. Thus lower gain and efficiency result from this current. Either a buffer layer of pure AlGaAs, as a barrier to electron flow, or excess chromium traps in the buffer substrate, or both, could substantially lower this parasitic current and are being pursued.

<u>Personnel Associated with this Task</u>

1. Lester F. Eastman, Principal Investigator
2. David W. Woodard, Senior Research Associate
3. Sandip Tiwari, Graduate Student
4. Michael Shur, Visiting Research Associate
5. John D. Berry, Technical Associate

Publications on this Task

"Design Criteria for GaAs MESFET's Related to Stationary High-Field Domains", M.S. Shur, L.F. Eastman, S. Judaprawira, J. Gammel, and S. Tiwari, IEDM Proceedings, Dec. 1978, "Substrate Currents in GaAs", L.F. Eastman and M. Shur, accepted for publication in IEEE trans, EDS.

Publications in Related Areas

"Surface Oriented Transferred-Electron Devices", M.S. Shur, and L.F. Eastman, IEEE trans, MTT, 26 (December 1978), "Rectification n-n GaAs: (Al,Ga)As Heterojunctions", A. Chandra and L.F. Eastman, Electronics Letters, 15, 3, 90-91, (February 1979)

Talks on this Task

"The Use of AlGaAs Buffer Layers to Reduce Parasitic Space Charge Limited Current Flow through Substrates in FET Structures", L.F. Eastman, D.W. Woodard, A. Chandra, and M. Shur, WOCSEMMAD, Atlanta, February 1979.

Talks on Related Areas

"Rectification at NGaAs NAlGaAs Heterogunctions Grown by LPE", by A. Chandra dn L.F. Eastman, Conference on Physics of Compound Semiconductor Interfaces, Asilomar, California, January 1979.

"Ballistic Electron Transport in Short Channel FET's", by M.S. Shur and L.F. Eastman, WOCSEMMAD, Atlanta, February, 1979.

"Current-Voltage Characteristics, Small Signal Parameters and Switching Times of GaAs FET's", M. Shur and L.F. Eastman, International Microwave Symposium, Ottawa, June 1978.

"Speed Limitations of GaAs Devices for Integrated Circuits", L.F. Eastman and M. Shur, Device Research Conference, Santa Barbara, California, June 1978.

Information/Technology Transfer

Both design and analysis of high power GaAs FET's done for the benefit of Westinghouse Research Laboratory (small subcontract on DARPA project), emphasizing high breakdown voltage and low substrate current-ongoing transfer.

Modeling of FET devices for logic done for the benefit of Rockwell Science Center (small subcontract on DARPA Project) emphasizing switching speed and computer aided circuit design-ongoing transfer.

Information/Technology Transfer (continued)

Modeling of FET devices for logic and microwave amplifiers, as well as contact and other device processing technology, for the benefit of IBM (contract funding for three years), initiated June 1979.

General Technology of devices, materials, processing and circuits transferred during L.F. Eastman Sabbatical 1978-1979.

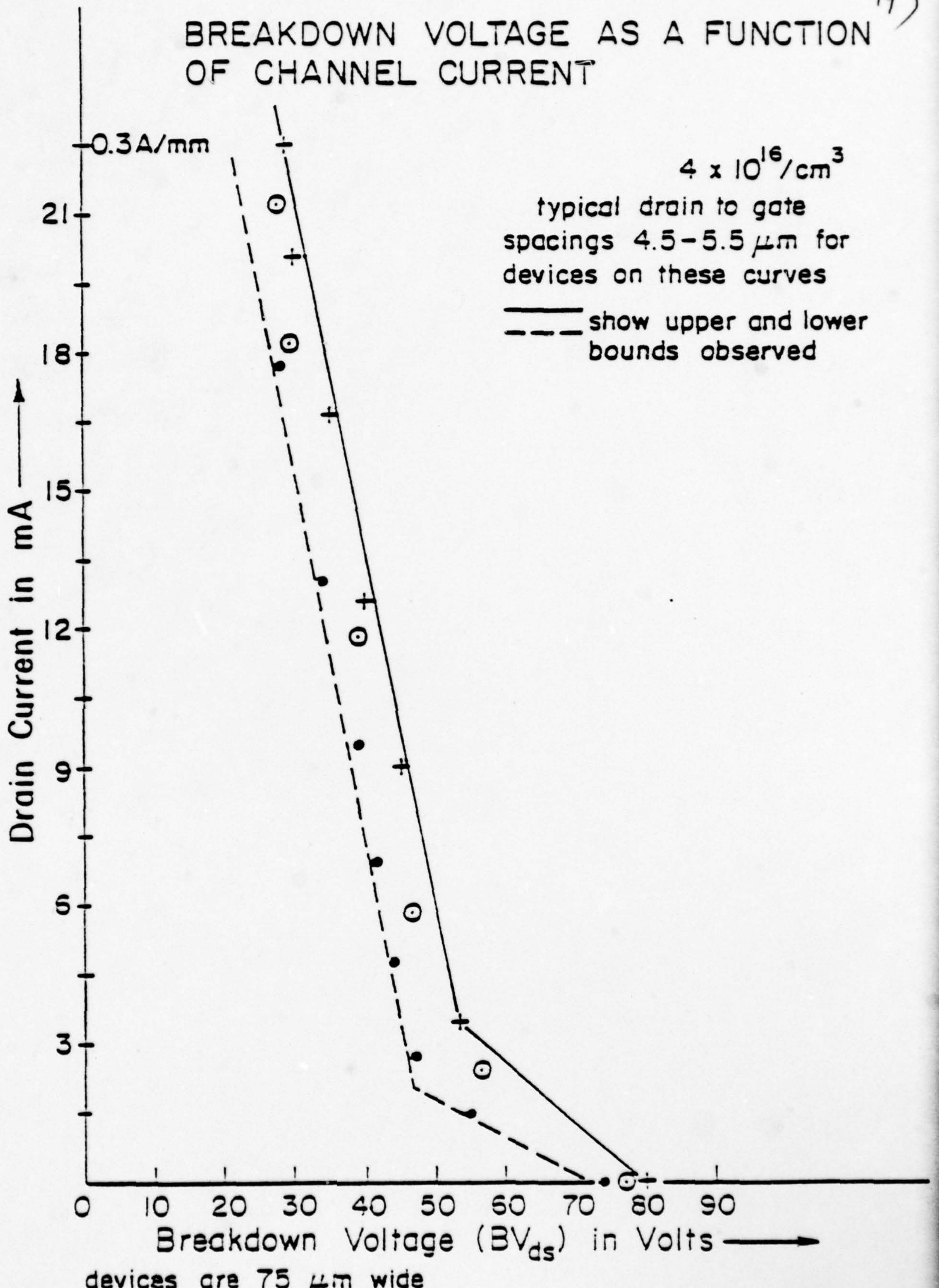
BREAKDOWN VOLTAGE AS A FUNCTION OF CHANNEL CURRENT
0.3A/mm
4 x 10^16/cm^3
typical drain to gate spacings 4.5-5.5 μm for devices on these curves
show upper and lower bounds observed
Drain Current in mA
21
18
15
12
9
6
3
0
10
20
30
40
50
60
70
80
90
Breakdown Voltage (BV_ds) in Volts
devices are 75 μm wide

Figure 3-1.

Task 4. Advanced Design Techniques for Microwave GaAs FET Amplifiers - Walter H. Ku

Progress

Significant progress was made on this unit of the Research Program on advanced design techniques for microwave GaAs FET amplifiers. An integrated design approach using analytical and computer-aided design (CAD) techniques has been fully developed for the design of wide classes of GaAs MESFET amplifiers. Significant contributions have been made toward the understanding of device-circuit interactions and derivations of explicit fundamental device-circuit limitations for micron and sub-micron gate-length GaAs MESFET's. Interactive computer programs have been developed for the synthesis of lumped and distributed matching networks for the design of broadband low-noise and high-power MESFET amplifiers. Using the distributed synthesis programs, matching networks are synthesized directly in distributed forms with arbitrarily prescribed gain slopes, bandwidth and impedance transformation ratio with exact tapered-magnitude maximally-flat and equiripple gain characteristics. To demonstrate the integrated design approach using distributed synthesis, FET amplifiers using 0.5 uM and 1.0uM gate-length MESFET's have been developed. Using the lumped synthesis program, broadband GaAs FET amplifiers can be designed in configurations which are suitable for monolithic realizations. The synthesis of lossy lumped matching networks is currently being investigated. Preliminary results show that low-noise and medium-power octave-band monolithic GaAs FET amplifier modules are feasible but a more detailed and systematic

design approach involving better models of the FET and the realizable matching elements is needed. It is anticipated that interactions of material, device, and circuit parameters will become even more important and design approaches similar to those used in conventional lower frequency IC design need to be developed for future monolithic microwave integrated circuits (MMIC) and subsystems.

An optimum design theory for broadband low-noise GaAs MESFET amplifiers has also been developed. The design theory is based on a simplified noise equivalent dircuit of the GaAs MESFET and analytical and computer-aided design techniques for broadband FET amplifiers. A simplified noise equivalent circuit of the GaAs MESFET together with the measured small-signal scattering parameters of the device is used to predict the noise figure versus frequency characteristics. An optimum gain slope and gain-bandwidth limitations are then derived for the input matching network of the low-noise amplifier. Synthesis techniques are then used to design the broadband low-noise MESFET amplifiers using 1 µm- and 0.5 µm-gate length GaAs FETs. For a typical 0.5 µm device with an assumed noise figure of 2 dB at 10 GHz, based on the simplified noise equivalent circuit, it is predicted that an input matching network with an approximate 4 dB/octave taper will provide an optimum noise match. Using this result, a 6-18 GHz MESFET amplifier can be designed to provide a flat noise figure of 3.2 dB $\pm$ 0.3 dB across the entire frequency band. Assuming a

typical circuit loss of 1 dB, the optimum design theory developed in this paper can be used to achieve a practical and realizable low-noise amplifier with noise figure less than 4.5 dB across the entire X- and Ku-band frequencies.

Publications on this Task

1. "An Adapting Delay Comb Filter Using Charge Transfer Devices", W. H. Ku, B. A. Hutchins and E. Kellett, paper presented at the 1978 IEEE International Symposium on Circuits and Systems, NY, NY, 17-19 May 1978.

2. "Techniques for Design, Test and Evaluation of GaAs FET Components for Phased Array Applications". Proceedings of the 1978 Military Microwave Conference, London, 25-27 October 1978.

3. "Ultra-Wideband GaAs MESFET Power Amplifier Designs for EW System Applications", W. H. Ku and H. A. Willing, Proceedings of 1978 Government Microcircuit Applications Conference (GOMAC), pp. 145-148, 14-16 November 1978.

4. "CTD Adaptive Filters for Interference Cancellation and Pitch Extraction", B. A. Hutchins and W. H. Ku, Proc. of Twelfth Asilomar Conference on Circuits, Systems, and Computers, November 1978.

List of Papers Accepted for Presentation:

1. "Synthesis of Distributed Networks and Their Applications to the Design of Microwave Solid-State Amplifiers", W. H. Ku. (Invited Paper), -- to be presented at the 1979 International Symposium on Circuits and Systems, Tokyo, Japan, 17-19 July

2. "Computer-Aided Design (CAD) of Microwave GaAs MESFET Amplifiers," W. H. Ku and W. C. Petersen, paper accepted for presentation at the Cornell Conference on Active Microwave Semiconductor Devices and Circuits, Ithaca, N.Y. August 14-16, 1979

3. "Optimum Design of Broadband Low-Noise MESFET Amplifiers," A. F. Podell, W. H. Ku and L.C.T. Liu, paper accepted for presentation at the Cornell Conference on Active Micromave Semiconductor Devices and Circuits, Ithaca, N.Y., August 14-16, 1979

List of Transfers of Technology, Ideas

1. Cooperative efforts on the design and fabrication of prototype medium-power GaAs MESFET amplifiers with Harry Willing and other members of the Microwave Technology Branch (Code 5250, Dr. Larry Whicker) of the Naval Research Laboratory (NRL)

2. Consulting for NRL and Naval Electronic Systems Command (NAVELEX) on microwave solid-state devices, circuits and subsystems.

3. Developed close relationships for exchange of technical information with Texas Instruments, Westinghouse and Varian on the design and characterizations of submicron gate FETs.

4. Consulting for NRL's Solid-State Devices Branch (Code 5210, Dr. John Davey) on the NAVELEX TRW Monolithic GaAs Program. The goal of this program is to develop a complete X-band monolithic GaAs chip using MESFETs and TEDs.

5. Serve on the DOD Technical Review Team for the DARPA/RADC Space Based Radar Module Program.

6. Consulting for DDRE (Larry Sumney) and ESD/XR (Dr. Donald Brick) on the signal processing portion (VHSIC-III) of the DOD VHSIC Program. Studied specifically high-speed high-throughput signal processing functions for various system applications.

7. Serving as Chairman of the Technical Committee on Computer-Aided Design (MTT Group 1) of the IEEE Microwave Theory and Techniques Society and Co-Chairman of the IEEE Circuits and Systems Society's Technical Committee on Optical, Microwave and Acoustical Circuits (OMAC).

8. CADSYN, an interactive computer program for the exact synthesis of distributed matching networks for microwave microstrip bipolar and GaAs MESFET amplifiers, has been introduced by COMPACT Engineering, Inc. in April 1979. This program was developed by Professor Ku and his former Research Assistant (supported by an NSF Grant and RADC/ET), Dr. Wendell C. Petersen of Varian Solid-State West. Over 70 companies are now using this program and Lincoln Lab. has purchased one version of CADSYN. A brief write-up of CADSYN and a User's Manual are available upon request.

TASK 5 Secondary Multiplication in Submicron Implanted Junctions in Relation to Improved Performance of Photomultipliers and Read Avalanche Diodes - Charles A. Lee

Status and Progress:

Measurements of the intrinsic avalanche response time and comparison with theory have been completed for silicon, GaAs including the crystal orientation dependence, germanium, and indium phosphide. This work has been terminated under the present contract.

Publications:

1. C. A. Lee, J. Berenz, and G. C. Dalman, "Determination of GaAs Intrinsic Avalanche Response Time from Noise Measurements, "Proceedings of the Sixth Biennial Cornell Conference on Active Microwave Semiconductor Devices and Circuits, p. 233-245, August 1977.

2. J. J. Berenz, J. Kinoshita, T. L. Hierl, and C. A. Lee, "Orientation Dependence of u-Type GaAs Intrinsic Avalanche Time", Electronics Letters 15, #5 pp. 150, 1 March 1979.

3. S. Basu, and C. A. Lee, "Compatibility of Ionization Rates and Intrinsic Response Time in Ge Junctions," To be submitted for publication. (Also MS Thesis - S. Basu)

Transfer of Technology

Raytheon Corporation: D. H. Statz, Dr. R. Bierig and Dr. R. Pucell have been the people with which most extensive contact has been made. There is and has been a continuous interaction concerning the evaluation of diodes and material- There is currently a Raytheon fellow, Glenn Thoren, who is pursuing doctoral research in mm-wave devices.

Varian Associates, Inc.: Principle contacts have been Dr. J. Berenz, Dr. T. Hierl, and Dr. Berin Fank. Measurements of orientation dependence of intrinsic response time in GaAs and response time measurements of InP have been carried out jointly.

SAMSO: Presented 4/26/79 (with G. C. Dalman) Major Chandler Kermedy successful results on a one diode eleven watt linear Impatt amplifier with 3 order intermodulation distortion of less than -15 dB below two tone carrier power.

Wright Patterson Avionics Lab: Presented 6/4/79 (with G.C. Calman to Dr. R. Kimmerly and Dr. R. Remski, linear amplifier results.

TASK 6 Design and Fabrication of High Efficiency Complimentary Read Type Silicon ($n^+p\pi p^+$) Diodes

Progress:

In a previous portion of this task, ion-implanted Si $p^+n\nu n^+$ Read structures has been fabricated and evaluated[1]. This work showed that the moderate efficiency obtained (9%) was due to a very small intrinsic response time which gave rise to an avalanche phase delay of 35° - 50° rather than the expected 85° - 90°. These diodes had material parameters which were quite similar to those made in several industrial laboratories which had similar moderate efficiencies.

From this analysis of the $p^+n\nu n^+$ structure the short intrinsic response time (~ .3 ps.) implied that electrons comprised the major component of the saturation current. It was conjectured that in the complimentary $n^+p\pi p^+$ diode holes would dominate the saturation current and thus the governing intrinsic response time would be that characteristics of holes, τ_{1p}. Ion-implanted $n^+p\pi p^+$ were fabricated and tested.[2] It was verified that the intrinsic response time was a factor of three times larger than the $p^+n\nu n^+$ structure and the avalanche phase delay was correspondingly improved to 80 - 85°. In spite of this improved avalanche phase delay the high power efficiency was still poor because of large parasitic resistance in the substrate. This work has been terminated under the present contract.

Publications:

1. Y. C. R. Kwor, C. A. Lee and G. C. Dalman, "Experimental and Theoretical Study of an Ion-Implanted Silicon Read IMPATT Diode", Submitted to Solid State Electronics (Also Ph.D. Thesis, Cornell University, Jan. 1976, R. Kwor).

Publications (continued)

2. A. K. Gupta, "Fabrication and Characterization of Ion-Implanted $n^+p\pi p^+$ Silicon Read IMPATT Diodes," Ph.D. Thesis, Jan. 1979, A. K. Gupta, Cornell University.

TASK 7 Large Signal Microwave FET and IMPATT Device-Circuit Interaction Studies - G. Conrad Dalman

Progress

Coaxial IMPATT reflection amplifiers using constant voltage bias have been built at X-band which have linear power output versus power input characteristics and low intermodulation distortion. The added power and efficiencies of these amplifiers are comparable to the oscillator results for the same devices. The advantages of using constant voltage bias is that the bias current rises with increasing input power preventing the gain from dropping at high input power levels. The best amplifier thus far has a maximum C.W. output power of 6.0 Watts, 3.1 dB gain and a corresponding third order intermodulation of -14 dB, neglecting circulator losses.

Admittance measurements as a function of r.f. input power were made on these amplifiers using a high power automatic network analyzer. This data is used to find the chip conductance and susceptance as a function of chip r.f. voltage. This data has contributed to an understanding of the origin of intermodulation distortion in linear amplifier applications.

Constant voltage amplifiers such as these could be a very attractive alternative to the travelling wave amplifier in communication systems.

List of Publications - none.

List of Papers Presented

"Linear High Power IMPATT Amplifiers Using Constant Voltage Bias", J.W. McClymonds, G.C. Dalman, and C.A. Lee, to be presented at 7th Biennial Conference Active Microwave Semiconductor Devices and Circuits, Cornell University August 14-16, 1979.

List of Transfers of Technology - none.

TASK 8 Development of Symmetry Analysis Methods for Periodic Structures - Paul McIsaac

Progress

The symmetry analysis of periodic waveguides with symmorphic space groups was developed. The analysis includes periodic structures containing:

1. axially magnetized gyrotropic media (e.g., ferrites),
2. a charged particle beam drifting parallel to the wave-guide axis.

The analysis procedure is based on the fact that for symmorphic space groups, the point group of symmetry operations is a subgroup of the space group.

The translation symmetry operations (parallel to the wave-guide axis) impose a Floquet form on the modal electromagnetic field functions. The infinite set of modes of the periodic structure can be classified into a set of mode classes; there is one mode class associated with each row of each irreducible representation of the point group (these have been tabulated for most point groups of interest). For periodic structures suitable for microwave and millimeter applications, the irreducible representations of the point group will be either one- or two-dimensional. Mode classes associated with one-dimensional irreducible representations contain non-degenerate modes, while a pair of mode classes associated with a two-dimensional irreducible representation contain mutually degenerate pairs of modes.

Each mode class is characterized by a basic azimuthal symmetry possessed by all the modal functions contained in it. The general form of the modal functions of each mode class can be obtained by applying the projection operator belonging to the associated irreducible representation to an arbitrary general function. Based on the characteristic modal function of a mode class, one can determine a minimum sector of the periodic wavequide which is necessary and sufficient to completely establish all of the modes of that mode class. All of these symmetry-based results for a periodic waveguide are obtained without having to find explicit solutions to a set of partial differential equations with their associated boundary conditions.

Publication

P.R. McIssac, "A General Reciprocity Theorem", IEEE Trans. Microwave Theory and Techniques, vol. MTT-27, pp 340-342, April 1979.

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Publication

P.R. McIssac, "A General Reciprocity Theorem", IEEE Trans. Microwave Theory and Techniques, vol. MTT-27, pp 340-342, April 1979.

TASK 9 Circuit Techniques for Active and Passive Distributed Parameter Systems - H. J. Carlin

Review of Progress:

A novel and extremely versatile technique of broad banding applicable to active and passive components[1] has been generalized and extended to new applications. The generalization now allows the general design of band-pass structures by permitting the designer to use an equalizer with a non-minimum reactance characteristics, if desired. This has resulted in a variety of very broad band microwave amplifier designs[2]. In addition, the method has been extended to non-linear circuit design in connection with the synthesis of broad band varactor tuned microwave oscillators[3].

References:

1. H. J. Carlin, "A New Approach to Gain-Bandwidth Problems," IEEE Trans VCAS-24, No 4, April 1977

2. H. J. Carlin and J. Komiak, "A New Method of Broad-Band Equalization Applied to Microwave Amplifiers", IEEE Trans. VMTT-27, pp 93-99, pp 170 - 175, February 1979

3. C. Rauscher and H. J. Carlin, "Generalized Technique for Designing Broadband Varactor Tuned Negative Resistance Oscillators". To be published in Int'l Journal of Circuit Theory and Applications.

Papers Presented:

1. H. J. Carlin, "A New Method of Broad Band Circuit Design". Invited speaker Plenary Session of Symposium "Constructive Approaches to Mathematical Models" Carnegie-Mellon U., July 1978.

2. H. J. Carlin, "A New Approach to Broad Banding" Colloquium at Case-Western Reserve University, October 5, 1978.

3. H. J. Carlin, "Broad Band Matching", Colloquium at University of Pennsylvania, October 27, 1978.

Transfer of Technology:

H. J. Carlin was informed by Professor Paul Penfield of MIT, that the broad banding we discussed now is being developed into a large program for use [specifics not known] by Lincoln Laboratory.